Electronic Version
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Claims

[c1] 1. A semiconductor device, the semiconductor device comprising:
a bump pad and a fuse pad over a wafer, wherein the fuse pad includes a burnt fuse pad having a gap for electrical isolation;
a dielectric layer, disposed substantially above the burnt fuse pad and filling the gap; and
a bump structure, disposed on the bump pad.

[c2] 2. The semiconductor device of claim 1, further comprising a passivation layer, which exposes the bump pad and a portion of the burnt fuse pad, wherein the dielectric layer is over the passivation layer, covers the exposed portion of the burnt fuse pad, and fills the gap.

[c3] 3. The semiconductor device of claim 1, wherein the dielectric layer includes one selected from the group consisting of Benzocyclobutene (BCB), Poly-Imide (PI), Nitride, SiN_3, Spin-On Glass (SOG), Spin-On Dielectric (SOD), SiO_x, and SiO_2.

[c4] 4 The semiconductor device of claim 1, wherein the bump structure includes:

an under ball metallurgy (UBM) layer to cover the exposed bump pad; and
a bump on the UBM layer.

[c5] 5. The semiconductor device of claim 1, wherein the semiconductor device comprises a memory device.

[c6] 6. A protection structure for preventing a burnt fuse pad from re-electrical connection in a semiconductor device, the semiconductor device includes a bump pad, a bump structure on the bump pad, and a fuse pad over a wafer, wherein the fuse pad includes the burnt fuse pad having a gap for electrical isolation, the protection structure comprising:
a dielectric layer, disposed substantially above the burnt fuse pad and filling the gap of the burnt fuse pad.

[c7] 7. The protection structure of claim 6, wherein the dielectric layer includes one selected from the group consisting of Benzocyclobutene (BCB), Poly-Imide (PI), Nitride, SiN_3, Spin-On Glass (SOG), Spin-On Dielectric (SOD), SiO_x, and SiO_2.

[c8] 8. The protection structure of claim 6, further comprising a passivation layer, which exposes the bump pad and a portion of the burnt fuse pad, wherein the dielectric layer is over the passivation layer, covers the exposed

portion of the burnt fuse pad, and fills the gap.

[c9] 9. The protection structure of claim 6, wherein the semiconductor device includes a memory device.